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GRAPHICS CONTROLLER IP CORE FOR EMBEDDED APPLICATIONS

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ABSTRACT

In today's scenario, it is a need in Embedded environment to have a touch screen based Graphics device. Any graphics device need to be controlled by a graphics controller. This paper presents a design and development of an RGB interface graphics controller that can be integrated with a 32 bit RISC processor on a FPGA platform. It supports, 16bpp, WQVGA 320 x 240 display resolution. The controller is having separate Text and Graphics Layer in which Text layer always overlays the Graphics layer. It supports multiple and customs 8x8 and 16x16 character fonts. Interface to the processor is through Industry standard high speed AMBA bus. It characterizes Double Frame Buffering technique for both Graphics and ASCII in which one buffer is updated based on the commands from the processor, while the other buffer throws the RGB data to the display glass in accordance to the pixel clock and horizontal and vertical synchronization signals. The final display buffer is updated from the 1st stage buffer during the vertical retrace period. A NOR Flash is interfaced to this graphics controller module so that images and customized fonts can be stored in it, that can be retrieved and played on the display glass as and when required. It can support 50 frames per second so that video can also be played seamlessly. This Graphics controller being a soft IP core and modular in design, hence it can be customized very easily for various types of such embedded display glasses. This is also very low gate count and very high performance graphics controller.

Keywords- 32 bit RISC processor, Soft IP core, AMBA bus, RGB interface, Double frame buffer

INTRODUCTION

The world is moving very fast towards small, handheld and battery operated application specific products from bulky PC based equipment and gadgets, and is present in every sphere of life, e.g, household, mobile phones, automobiles, car navigation etc. Embedded systems technology has an instrumental role to play in this emerging field. To provide visual information to the users, an integrated display is the basic needs of any such gadgets. The display or graphics controller provides the bridge between a graphics display and a processor[1].

In electronic design a semiconductor intellectual property core(IP core) or IP block is a reusable unit of logic, cell, or chip layout design that is the intellectual property of one party. IP core is of two types, Soft and Hard. Soft IP cores are typically offered as synthesizable RTL and delivered in a hardware description language such as Verilog or VHDL. Soft IP cores are also sometimes offered as generic gate-level netlists. Whereas, Hard IP core is fully designed, placed and routed file. It is a physical layout of a design and of fixed shape, and hence tied to a manufacturing process and has no flexibility [2,3].

This paper describes the design and development of a graphics controller soft IP core, to be used with a custom 32-bit RISC processor whose instruction set architecture is compatible to that of an open source 32-bit GNU compiler tool chain. This processor and the Graphics IP core are implemented on a Xilinx Kintex-7 FPGA platform. The development was done in Xilinx ISE 14.6 environment and the language used was VHDL. The tools used for simulation and testing are Xilinx Isim, Xilinx Chip scope Pro and Mentor Graphics Modelsim.